

Form PTO-1449 U.S. DEPARTMENT OF
COMMERCE PATENT AND
TRADEMARK OFFICEATTY DOCKET NO.
0325.00417SERIAL NO.
09/668,801INFORMATION DISCLOSURE
STATEMENT BY APPLICANTAPPLICANT:
Timothy J. WilliamsFILING DATE
September 22, 2000GROUP
2188

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.							Date	Name	Class	Sub- Class	Filing Date
<i>C</i>	4	6	8	9	7	4	0	8/25/1987	Moelands et al.	364	200	
<i>C</i>	5	5	5	9	5	0	2	9/24/1996	Schutte	340	825.21	
<i>C</i>	5	6	8	9	1	9	6	11/18/1997	Schutte	326	86	

FOREIGN PATENT DOCUMENTS

	Document No.							Date	Country	Class	Sub- Class	Transl.	
												Yes	No
<i>C</i> WO 99	/	0	9	7	1	2		25.02.1999	PCT	H04L 12/40		X	
<i>C</i> WO 96	/	1	7	3	0	5		06.06.1996	PCT	G06F 13/40, 1/32		X	
<i>C</i> WO 98	/	3	4	3	7	6		06.08.1998	PCT	H04L 12/20		X	

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)

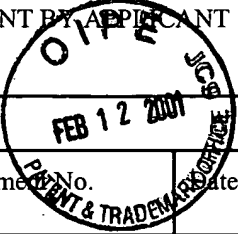
Examiner

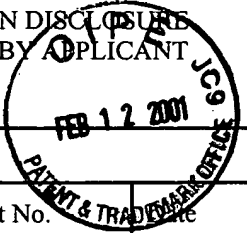
CAO


Date Considered

5/3/04

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U.S. PATENT DOCUMENTS						
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C	4 0 6 1 9 8 7	12/6/1977	Nagahama	331	111	
	4 2 7 2 7 6 0	6/9/1981	Prazak et al.	340	347	
	4 3 4 4 0 6 7	8/10/1982	Lee	340	347	
	4 6 9 2 7 1 8	9/8/1987	Roza et al.	331	113R	
	4 8 6 8 5 2 5	9/19/1989	Dias	331	111	
	4 9 4 7 1 6 9	8/7/1990	Smith et al.	341	121	
	5 1 4 0 1 9 7	8/18/1992	Grider	307	480	
	5 1 5 0 0 7 9	9/22/1992	Williams et al.	331	75	
	5 1 7 5 8 8 4	12/29/1992	Suárez	455	260	
	5 2 0 0 7 5 1	4/6/1993	Smith	341	147	
	5 3 0 4 9 5 5	4/19/1994	Atriss et al.	331	1R	
C	5 3 1 9 3 7 0	6/7/1994	Signore et al.	341	120	
FOREIGN PATENT DOCUMENTS						
	Document No.	Date	Country	Class	Sub-Class	Transl. Yes No
OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)						
C	A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2- μ m CMOS, By: Beomsup Kim et al., Journal of Solid-State Circuits, Vol. 25, No. 6, December 1990, pages 1385-1394.					
a	WP 3.5: An Integrated Time Reference, By: Robert A. Blauschild, ISSCC94/Session 3, Analog Techniques/Paper WP 3.5, 1994.					
C	Micropower CMOS Temperature Sensor with Digital Output, By: Anton Bakker et al., 1996 IEEE.					
a	CY7C63722/23 CY7C63742/43 enCoRe™ USB Combination Low-Speed USB & PS/2 Peripheral Controller, Cypress Semiconductor Corp., February 2000 - Revised April 11, 2000, pages 1-51.					
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT 		RECEIVED FEB 13 2001 Technology Center 2100			
		APPLICANT: Timothy J. Williams		FILING DATE September 22, 2000	
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U.S. PATENT DOCUMENTS					
Examiner Initial	Document No.	Date	Name	Class	Sub- Class
C	5 4 2 8 3 1 9	6/27/1995	Marvin et al.	331	176
1	5 4 4 0 3 0 5	8/8/1995	Signore et al.	341	120
1	5 5 4 6 4 3 3	8/13/1996	Tran et al.	375	376
1	5 5 5 2 7 4 8	9/3/1996	O'Shaughnessy	331	1A
1	5 5 6 3 5 5 3	10/8/1996	Jackson	331	57
1	5 5 6 5 8 1 9	10/15/1996	Cooper	331	111
1	5 5 8 3 5 0 1	12/10/1996	Henrion et al.	341	118
1	5 5 9 4 6 1 2	1/14/1997	Henrion	341	120
1	5 6 0 4 4 6 6	2/18/1997	Dreps et al.	331	113R
1	5 6 6 6 1 1 8	9/9/1997	Gersbach	341	120
1	5 6 6 8 5 0 6	9/16/1997	Watanabe et al.	331	66
C	5 6 7 0 9 1 5	9/23/1997	Cooper et al.	331	111
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	Document No.	Date	Country	Class	Sub- Class
OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)					
C	An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance, By: Sam Yinshang Sun, Reprinted from IEEE Journal of Solid-State Circuits, Vol. SC-24, pp. 325-330, April 1989.				
C	CY7C63221/31 enCoRe™ USB Low Speed USB Peripheral Controller, Cypress Semiconductor Corp., February 2000 - Revised April 11, 2000, pages 1-43.				
C	Timothy J. Williams et al., "AUTO-LOCKING OSCILLATOR FOR DATA COMMUNICATIONS", U.S. Serial No. 09/511,019, Filed February 23, 2000.				
C	Timothy J. Williams et al., "CIRCUIT FOR LOCKING AN OSCILLATOR TO A DATA STREAM", U.S. Serial No. 09/511,020, Filed February 23, 2000.				
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C	5	6	8	2	0	4	9	10/28/1997	Nguyen	257	363			
	5	6	8	6	8	6	3	11/11/1997	Whiteside	330	260			
	5	7	2	6	5	9	7	3/10/1998	Petty et al.	327	307			
	5	7	9	6	3	1	2	8/18/1998	Hull et al.	331	44			
	5	8	1	8	3	7	0	10/6/1998	Sooch et al.	341	120			
	5	8	2	5	3	1	7	10/20/1998	Anderson et al.	341	120			
	5	8	9	8	3	4	5	4/27/1999	Namura et al.	331	177V			
	6	1	5	7	2	6	6	12/5/2000	Tsai et al.	331	57			
	5	3	4	5	1	9	5	9/6/1994	Cordoba et al.	331	111			
	5	6	9	9	0	2	4	12/16/1997	Manlove et al.	331	111			
	5	8	7	0	0	0	4	2/9/1999	Lu	331	176			
C	5	8	7	0	3	4	5	2/9/1999	Stecker	365	222			
FOREIGN PATENT DOCUMENTS														
	Document No.							Date	Country	Class	Sub- Class	Transl. Yes No		
OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)														
C	Universal Serial Bus Specification, Revision 2.0, April 27, 2000, pp. 1-622.													
C	Monte F. Mar et al., "PROGRAMMABLE OSCILLATOR SCHEME", U.S. Serial No. 09/721,316, Filed November 22, 2000.													
C	Monte F. Mar et al., "PROGRAMMABLE OSCILLATOR SCHEME", U.S. Serial No. 09/275,336, Filed March 24, 1999.													
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